CS 220

The MIPS Instruction Pipeline – Part 2

Reading memory

Analyze a data dependency with a **lw** instruction.

```
lw t0, 0(sp)

add t1, t0, t0
```
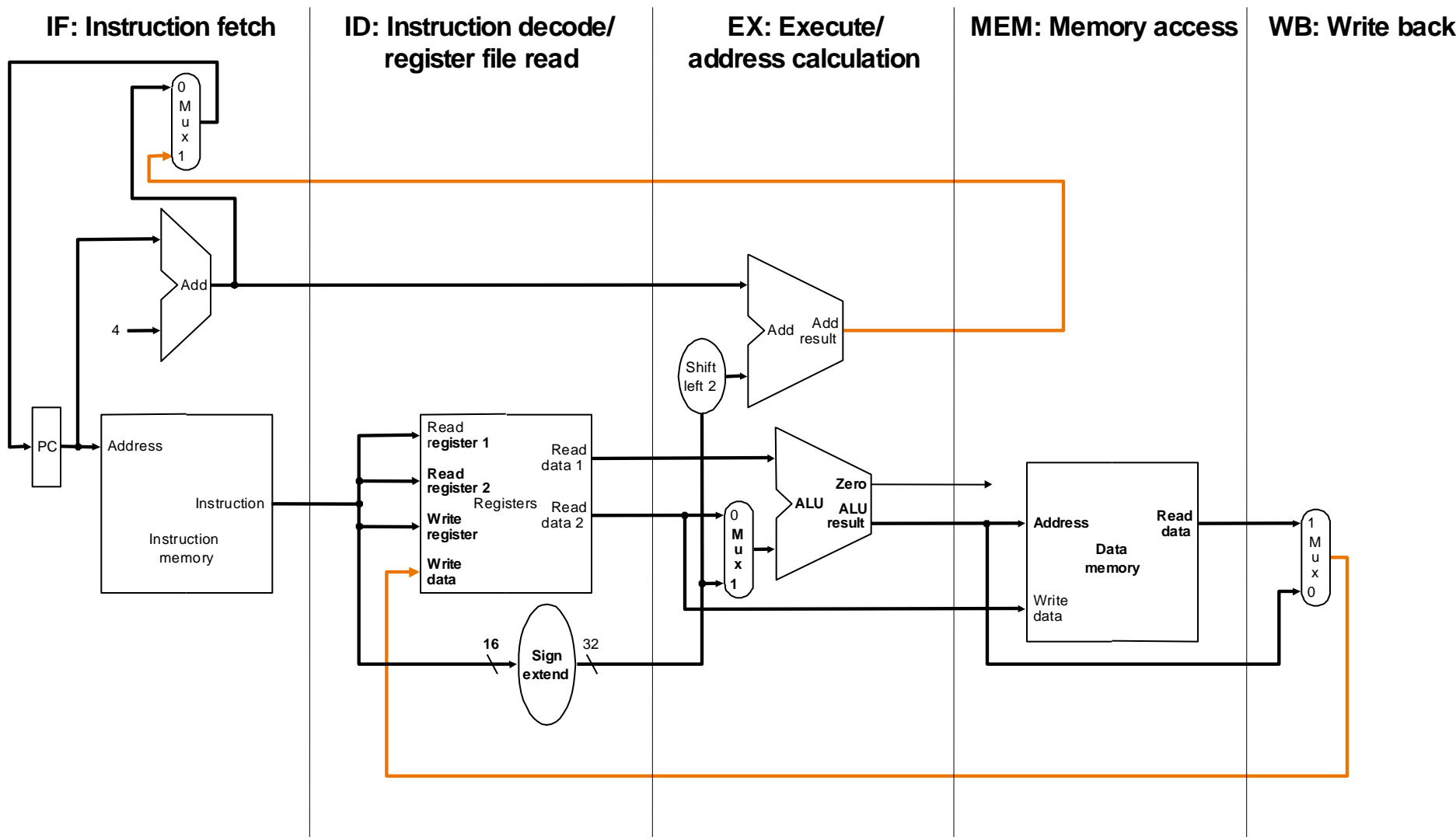
Solutions?

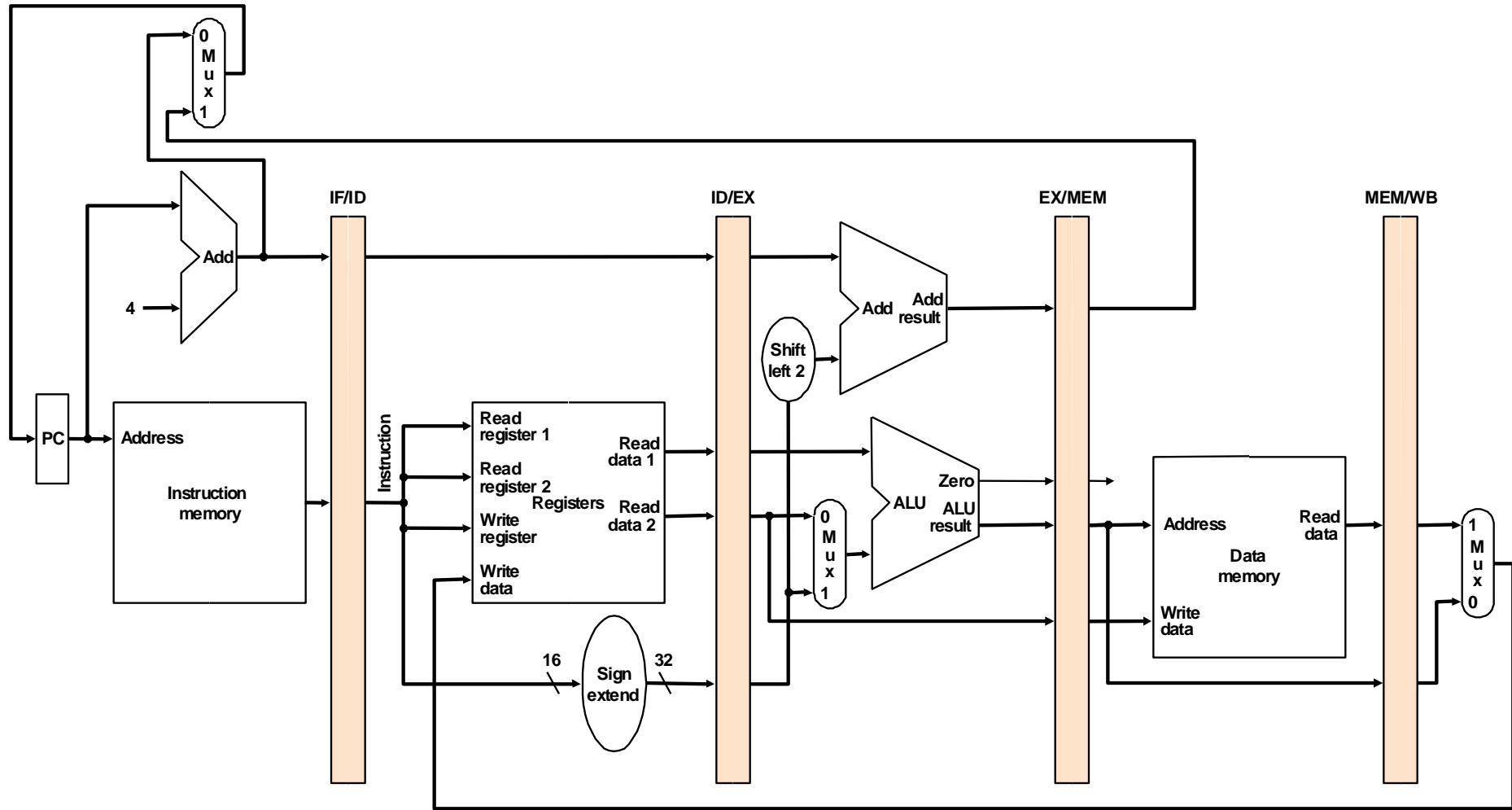# Can we minimize stalling?

```
A  =  B  +  E
C  =  B  +  F
```

Assuming these variables are stored in memory write the MIPS code for these statements.

Control Hazard: MIPS Solution

```
loop:
      addi $t0, $t0, -1
      bne $t0, $zero, loop
      ori $v0, $zero, 9
      add $t3, $t4, $t5
```

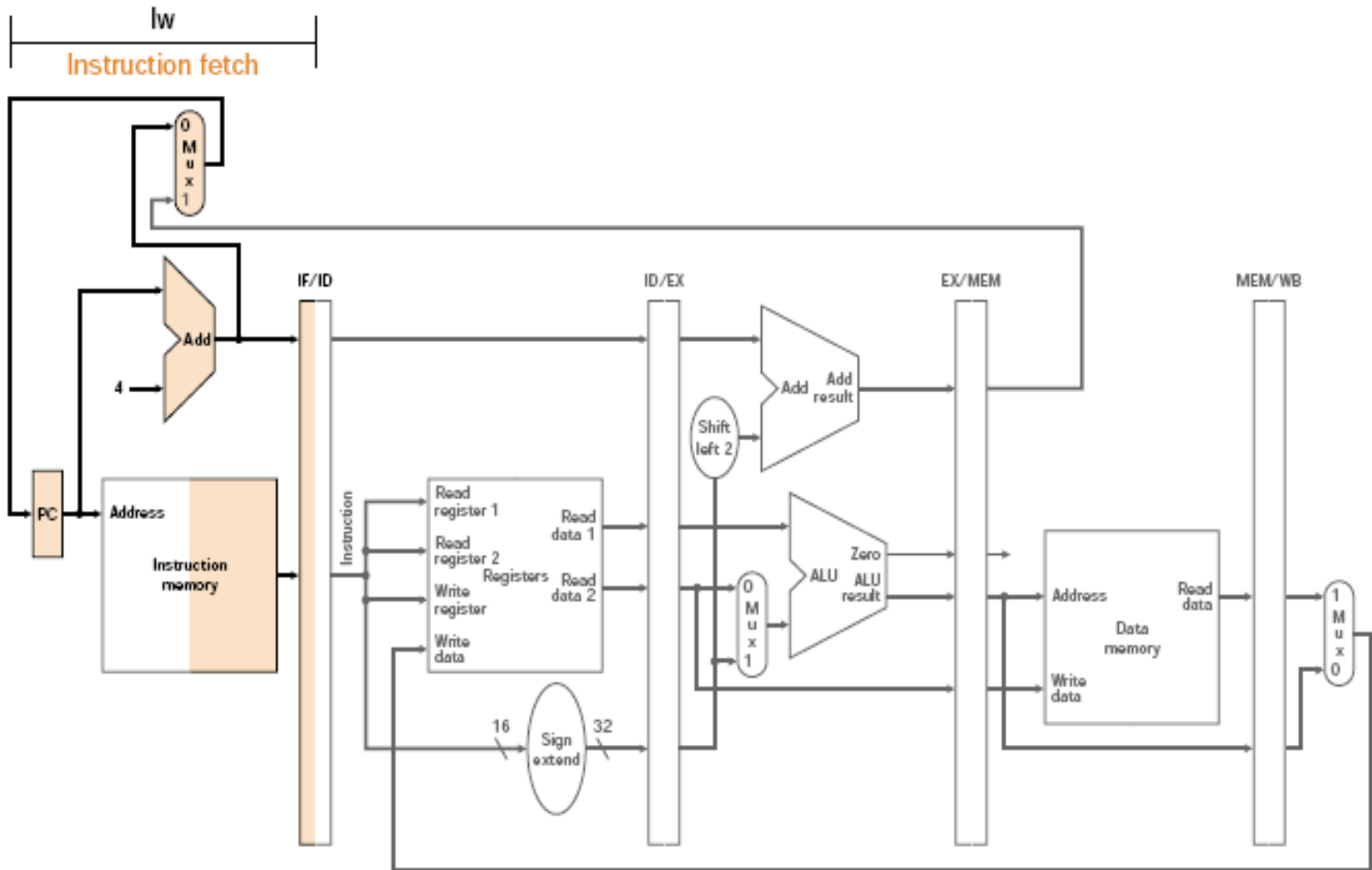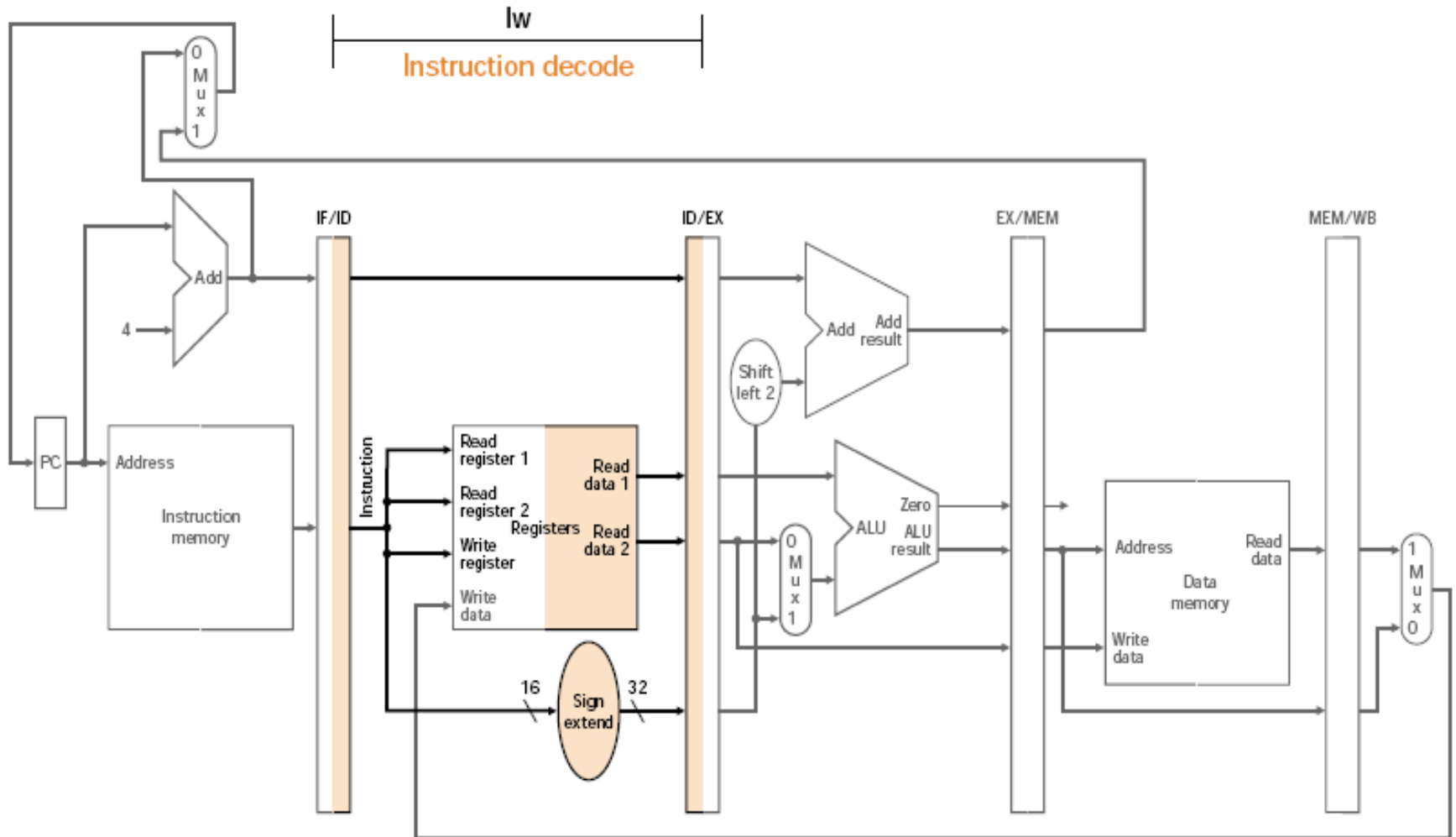|								

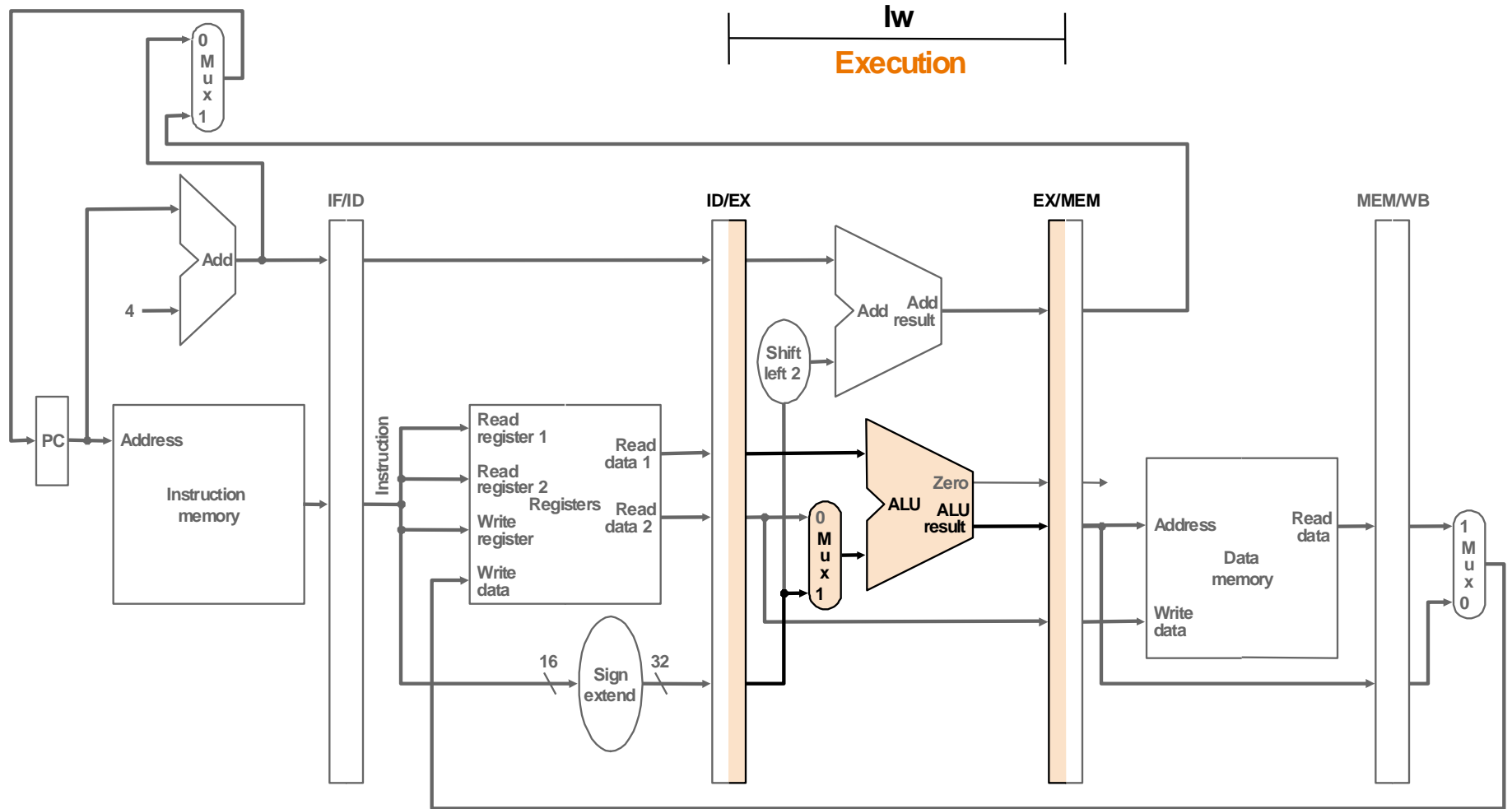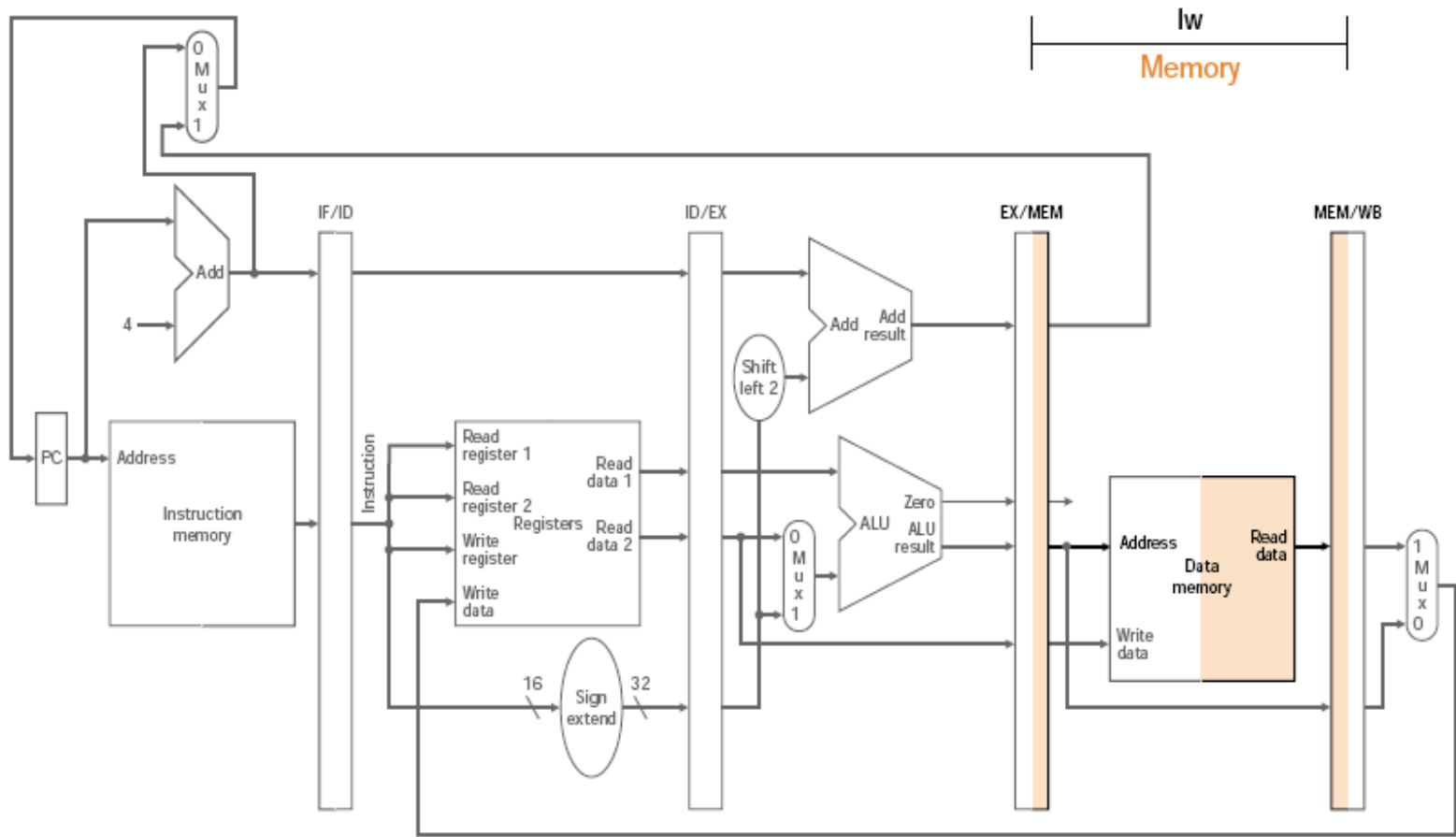# Pipelined Datapath

Pipelined Datapath
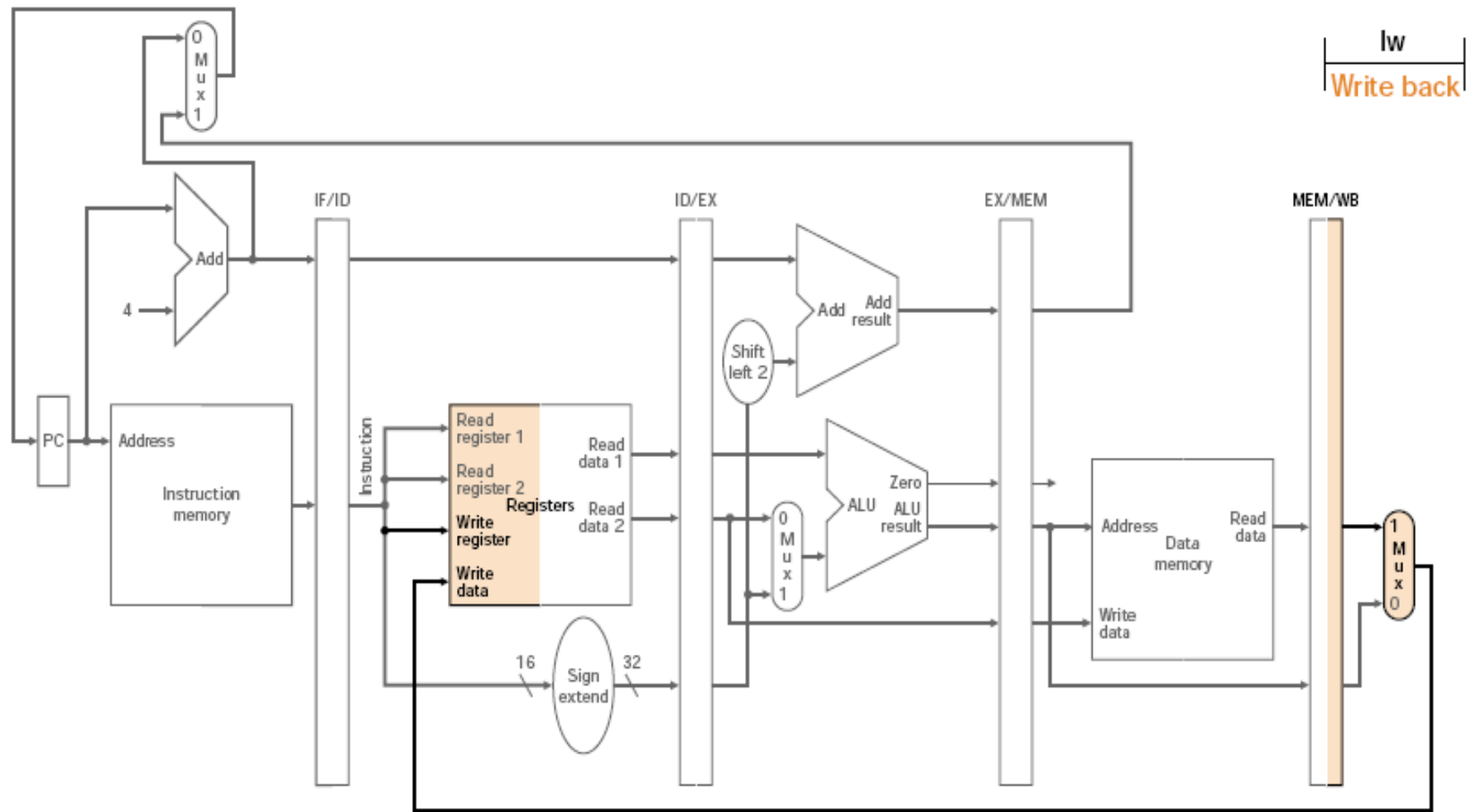
Tracing a LW instruction

Tracing a LW instruction

Tracing LW: EX

LW: Memory

LW: Writeback

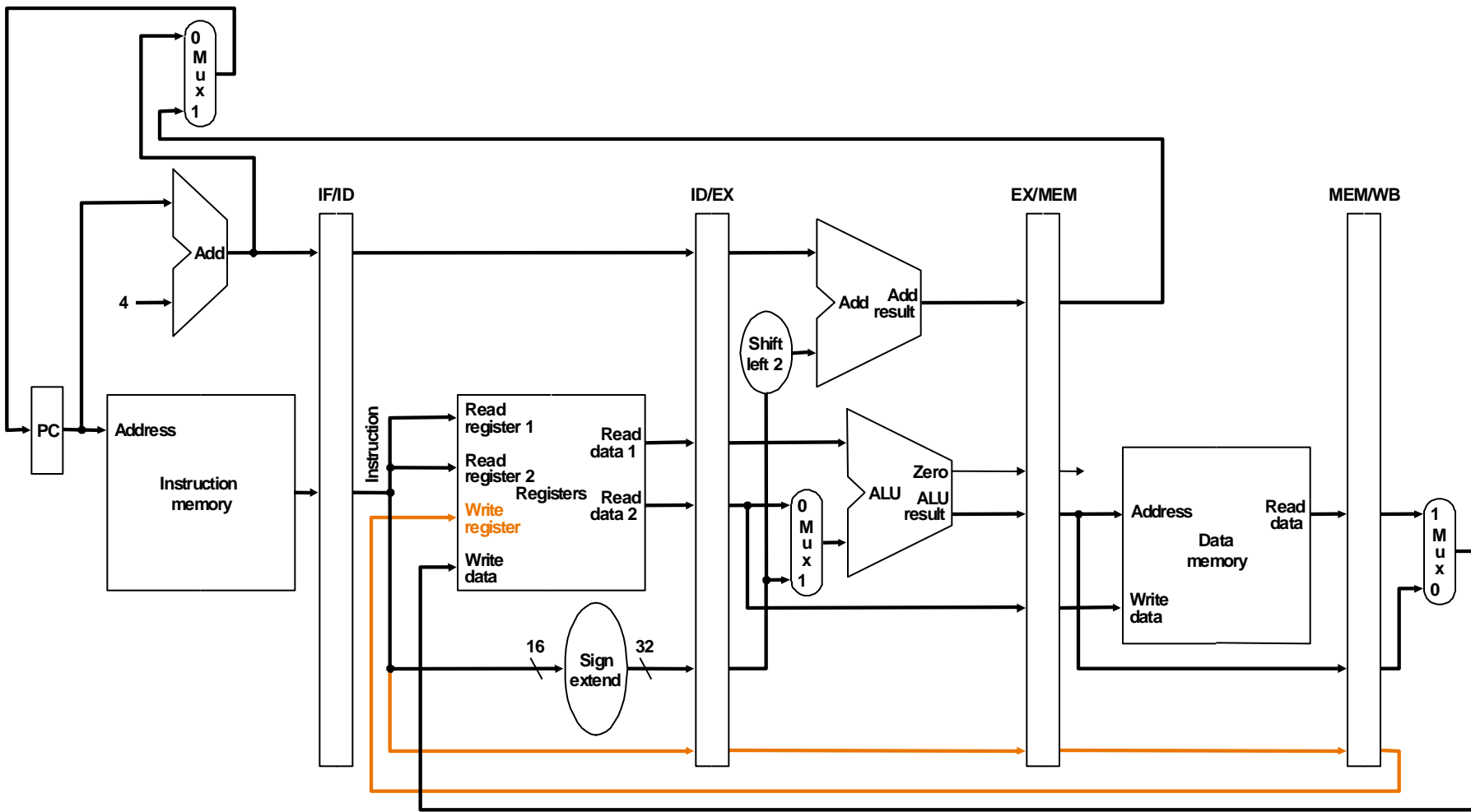Figures are © Morgan-Kauffman Publishers 2010

Problem?

lw Writeback: bug fixed

Pipelined Datapath w/Control Signals